IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF:
YIN TAT MA
SERIAL NO. : 10/501,651

FILED: JANUARY 10, 2005

FOR: ON-CHIP ESD PROTECTION CIRCUIT FOR COMPOUND SEMICONDUCTOR HETEROJUNCTION BIPOLAR TRANSISTOR RF CIRCUITS

Examiner: D. H. PATEL

Group Art Unit: 2836

COMMUNICATION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In reply to the Office communication mailed May 11, 2006, enclosed are two drawings with each drawing page identified in the top margin as "Replacement Sheet".

If there are any additional charges for this case, please charge Deposit Account No. 01-1960.

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on May 23, 2006 by Jo Ann Breen.

Signature

May 23, 2006

Respectfully submitted,

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